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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/731,385	12/09/2003	Tae-Sik Oh	51345/DBP/Y35	4675

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EXAMINER	
ROY, SIKHA	
ART UNIT	PAPER NUMBER
2879	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/26/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/731,385	OH, TAE-SIK	
	Examiner	Art Unit	
	Sikha Roy	2879	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20 and 23-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20 and 23-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

The Amendment, filed on October 11, 2006 has been entered and acknowledged by the Examiner.

Cancellation of claims 21,22 has been entered.

Claims 1-20 and 23-25 are pending in the instant application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 9, 12, 15,16 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 5,965,978 to Kishino et al.

Regarding claim 9 Kishino discloses (Fig. 3 column 4 lines 9-40, column 5 lines 1-11) a first substrate 3 and a second substrate 2 opposing one another with a predetermined gap there between, the first substrate and second substrate being sealed using a sealant (low melting point glass hermetically bonding substrates 2,3) thus forming a vacuum assembly, an electron emission assembly formed on the first substrate and emitting electrons by generation of electric fields within the electron emission assembly, an illumination assembly formed on the second substrate and realizing a display of images by electrons emitted from the electron assembly, wherein

the illumination assembly includes a phosphor screen formed on the surface of the second substrate, a metal layer 6 formed on the phosphor screen within the vacuum assembly and an anode input terminal 6a formed extending from within the vacuum assembly to outside the sealant in which the end of the anode input terminal 6a within the vacuum assembly contacts the metal layer 6 to be electrically connected to the metal layer and an anode voltage is applied to a portion of the anode input terminal through the lead 28 extending beyond the sealant.

Regarding claim 12 Kishino discloses (Fig.1b column 4 lines 50-67) the electron emission assembly includes electron sources 15 and electrodes for inducing emission and wherein the electrodes include cathode electrodes 11 and the gate electrodes 13, being insulated from each other by an insulation layer and formed in a stripe pattern, the cathode electrodes being perpendicular to the gate.

Regarding claim 15 Kishino discloses the cathode electrodes formed on the first substrate 3, the insulation layer 12 formed on the first substrate covering the cathode electrodes, the gate electrodes 13 formed on the insulation layer , the insulation layer and the gate electrodes having openings for exposing the cathode electrodes and the electron emission sources 15 being formed in the openings on the exposed cathode electrodes.

Regarding claim 16 Kishino discloses (Fig.3) a flat panel display comprising a faceplate 2 including a faceplate interior side, a backplate 3 including a backplate interior side opposed to the face plate, sidewalls 4 positioned between the faceplate and the back plate to form an enclosed vacuum envelope between the side walls,

aphosphor layer 5 positioned on the faceplate interior side, a metal layer 6 positioned on the phosphor layer wherein the metal layer is formed entirely within the vacuum envelope and an anode input terminal 6a extends from within the vacuum envelope to outside the side walls.

Regarding claim 18 Kishino discloses (Fig.3) the metal layer 6 contacts the anode input terminal 6a within the vacuum envelope and an anode voltage is applied to the anode input terminal 6a outside the walls.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5,8 and 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,410,101 to Jaskie et al., and further in view of U.S. Patent 5,65,978 to Kishino et al.

Regarding claim 1 Jaskie discloses (Figs.1,3 column 2 lines 18-34, column 3 lines 31-67) a field emission device 120 comprising a first substrate 101 and a second substrate 122 opposing one another with a predetermined gap there between, the first substrate and the second substrate being sealed, an electron emission assembly 110

formed on the first substrate and emitting electrons by generation of electric fields within electron emission assembly and an illumination assembly 100 formed on the second substrate including a transparent conductive layer 124 formed on the surface of the second substrate and having an anode input terminal to which an anode voltage 118 is applied, a phosphor screen 126 formed on the transparent conductive layer and a metal layer (reflective layer)128 formed on the screen within the vacuum assembly a portion of the metal layer 128 contacting and electrically connecting the transparent conductive layer 124.

Jaskie does not explicitly disclose the substrates sealed by sealant forming the vacuum assembly and the transparent conductive layer having a portion extending beyond the sealant to which anode voltage is applied.

Kishino in same field of endeavor discloses (Fig.3 abstract) the first and second substrates 3,2 sealed using a sealant wherein a vacuum is formed between the two substrates and the anode input terminal formed on the anode substrate is extended beyond the sealant to which anode voltage is applied through the anode lead 28. Kishino teaches this configuration secures good electric conduction between the anode input terminal and the anode lead and uses easy-to-use anode leads.

Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to modify the transparent conductive layer 124 of Jaskie having an anode input terminal extending outside the sealant to which anode input voltage is applied, as shown by Kishino for securing good electric conduction between the anode input terminal and the anode lead.

Regarding claim 2 it is evident from Fig. 3 of Jaskie that the transparent conductive layer 124 and the anode input terminal connecting the anode voltage 118 are integrally formed.

Regarding claim 3 Jaskie discloses (column 2 lines 24,25) the transparent conductive layer and the anode terminal are made of indium tin oxide.

Regarding claim 4 it is evident from Fig. 3 the metal layer 128 is formed over the phosphor screen having an area larger that the phosphor screen such that the edges of the metal layer 128 contact the transparent conductive layer 124.

Regarding claim 5 Jaskie discloses (Fig. 3 column 3 lines 41-51) the electron emission assembly includes electron emission sources (emitter structure) 105 and electrodes for inducing emission of electrons from the emitters wherein the electrodes include the cathode electrodes 102 and gate electrodes 106 insulated from each other by an insulating layer 103 and formed in respective stripe patterns the cathode electrodes being substantially perpendicular to the gate electrodes.

Regarding claim 8 Jaskie discloses (Fig. 3) the cathode electrodes 102 are formed on the first substrate 101, the insulation layer 103 are formed on the first substrate covering the cathode electrodes and the gate electrodes 106 (107,108) are formed on the insulation layer the insulating layer and the gate electrodes having openings for exposing the cathode electrodes and the emission sources (emitters), the emitters being formed in the openings on the exposed cathode electrodes.

Regarding claim 23 Jaskie in view of Kishino disclose an illumination assembly for a field emission display comprising a substrate, a transparent conductive layer formed on the surface of the substrate, the transparent conductive layer having a portion extending beyond the sealant and having anode input terminal as a portion of the transparent conductive layer extending beyond the sealant to which anode voltage is applied, a phosphor screen formed on the transparent conductive layer and a metal layer formed on the phosphor screen and having a portion of the metal layer electrically contacting the transparent conductive layer within the vacuum assembly.

Claims 24 and 25 essentially recite the same limitations as of claims 2 and 4 respectively and hence are rejected for the same reasons (see rejection of claims 2 and 4).

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,965,978 to Kishino et al.

Regarding claim 11 Kishino discloses the claimed invention except the metal layer covering a portion of the anode input terminal. It would have been an obvious matter of design choice to have the metal layer covering a part of the anode input terminal since the applicant has not disclosed that this configuration of the metal layer solves any stated problem or is for any particular purpose and it appears that the invention would perform equally well with the metal layer connected to the anode input terminal as disclosed by Kishino.

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,965,978 to Kishino et al. and further in view of U.S. Patent 6,900,066 to Toyota et al.

Regarding claim 13 Kishino is silent about the electron emission sources made of carbon nanotube, graphite, diamond or combination of these materials.

Toyota in analogous art of field emission devices discloses (column 20 lines 13-25) the electron emission materials formed from carbon and diamond. Toyota teaches these material have large secondary electron gain and thus would enhance the field emission display.

Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to specify the electron emission sources of Kishino made of carbon and diamond as taught by Toyota for providing large secondary electron gain.

Claim 10,17,19,20 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,965,978 to Kishino et al. and further in view of U.S. Patent 6,410,101 to Jaskie et al.

Regarding claim 10 Kishino does not disclose the anode input terminal formed of material selected from a group consisting of indium tin oxide, Ni or Cr.

Jaskie discloses (column 2 lines 24, 25) the anode input terminal integrally formed with the transparent conductive layer formed of indium tin oxide. It is to be noted that this configuration provides simple manufacturing of the anode input terminal.

Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to modify the anode input terminal of Kishino with a transparent conductive layer and the input terminal made of indium tin oxide as taught by Jaskie for providing simple manufacturing of the display device.

Regarding claim 17 Kishino does not exemplify the metal layer 6 having larger area than the phosphor layer 5.

Jaskie discloses in Fig. 2 that the metal layer 128 has larger area than the separate phosphor layers 126 formed for different pixels.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the phosphor layer of Kishino by three separate phosphor layers and the metal layer having larger area than the phosphor layer as disclosed by Jaskie for providing emission from different pixels.

Regarding claim 19 Jaskie discloses a transparent conductive layer 124 formed between the faceplate and the phosphor layer.

Regarding claim 20 Kishino and Jaskie disclose the anode voltage is applied to the transparent conductive layer through the anode input terminal outside the sidewalls.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,410,101 to Jaskie et al., U.S. Patent 5,65,978 to Kishino et al. and further in view of U.S. Patent 6,900,066 to Toyota et al.

Regarding claim 6 Jaskie is silent about the electron emission sources made of carbon nanotube, graphite, diamond or combination of these materials.

Toyota in analogous art of field emission devices discloses (column 20 lines 13-25) the electron emission materials formed from carbon and diamond. Toyota teaches these material have large secondary electron gain and thus would enhance the field emission display.

Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to specify the electron emission sources of Jaskie and Kishino made of carbon and diamond as taught by Toyota for providing large secondary electron gain.

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,410,101 to Jaskie et al., U.S. Patent 5,965,978 to Kishino et al., and further in view of U.S. Patent 5,726,530 to Peng.

Regarding claim 7 Jaskie and Kishino do not disclose the gate electrodes being formed on the first substrate and the insulation layer being formed on the first substrate covering the gate electrodes.

Peng in the same field of endeavor discloses an FED comprising a substrate, a plurality of gate electrodes formed on the substrate, an insulation layer covering the gate electrodes, and a plurality of cathode electrodes over the insulating layer, and teaches this embodiment to be preferred over an FED wherein the cathode electrodes are disposed over the substrate, because the former provides a display whose

resolution is not limited by the provision of individual ballast resistors for each pixel, said ballast resistors having high reliability, being capable of meeting tight tolerance, and controlling the emission current of each pixel', and further the chances of short circuiting the display and its detrimental effects are reduced (see Col. 1, lines 43-60; Col. 2, lines 47-59; and Figs. 3A, 4A, 6A, 7A and 8A).

Thus, it would have been obvious to one of ordinary skill in the art at the time of invention to provide a plurality of gate electrodes on the first substrate and insulation layer covering the gate electrodes and a plurality of cathode electrodes over the insulating layer as taught by Peng for the field emission device of Jaskie for providing a display whose resolution is not limited by the provision of individual ballast resistors for each pixel, said ballast resistors having high reliability, being capable of meeting tight tolerance, and controlling the emission current of each pixel, and further the chances of short circuiting the display and its detrimental effects are reduced.

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,965,978 to Kishino et al. and further in view of U.S. Patent 5,726,530 to Peng.

Regarding claim 14 Kishino does not disclose the gate electrodes being formed on the first substrate and the insulation layer being formed on the first substrate covering the gate electrodes.

Peng in the same field of endeavor discloses an FED comprising a substrate, a plurality of gate electrodes formed on the substrate, an insulation layer covering the gate electrodes, and a plurality of cathode electrodes over the insulating layer, and

teaches this embodiment to be preferred over an FED wherein the cathode electrodes are disposed over the substrate, because the former provides a display whose resolution is not limited by the provision of individual ballast resistors for each pixel, said ballast resistors having high reliability, being capable of meeting tight tolerance, and controlling the emission current of each pixel', and further the chances of short circuiting the display and its detrimental effects are reduced (see Col. 1, lines 43-60; Col. 2, lines 47-59; and Figs. 3A, 4A, 6A, 7A and 8A).

Thus, it would have been obvious to one of ordinary skill in the art at the time of invention to provide a plurality of gate electrodes on the first substrate and insulation layer covering the gate electrodes and a plurality of cathode electrodes over the insulating layer as taught by Peng for the field emission device of Kishino for providing a display whose resolution is not limited by the provision of individual ballast resistors for each pixel, said ballast resistors having high reliability, being capable of meeting tight tolerance, and controlling the emission current of each pixel, and further the chances of short circuiting the display and its detrimental effects are reduced.

Response to Arguments

Applicant's arguments with respect to claims 1,9,16 and 23 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. U.S. Patent 5,955,832 to Tomita et al. discloses in Fig. 7 anode input terminal extending from the transparent anode outside the seal region.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sikha Roy whose telephone number is (571) 272-2463. The examiner can normally be reached on Monday-Friday 8:00 a.m. – 4:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimeshkumar D. Patel can be reached on (571) 272-2457. The fax phone number for the organization is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Sikha Roy

Sikha Roy
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12/20/06
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